Prof Rajeevan Chandel 28/11/2023

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(113)

National Institute of Technology Hamirpur (HP)

Name of Examination: END-SEMESTER EXAMINATION, 22 November 2023

Branch: Dual Degree Integrated E&CE, 4th Year — **Semester** : 7th

Course Name: Device Modeling for Circuit Simulation — **Course Code** : EC-631

Time: 3 Hours — **Maximum Marks: 50**

Room: F1/F2/F3, Session B: 2.30pm to 5.30pm

Note:

i) All questions are compulsory. Assume any missing data. ii) Give short answers for Q1.
iii) Attempt all parts of any question at one place & in sequence.

Q#		Questions	Marks	CO
1.	(i)	Design a MOSFET for attaining minimal threshold voltage?	2	CO1
	(ii)	Give significance and meaning of Early effect and high level injection in electronic diodes and transistors?	2	
	(iii)	Write SPICE commands for a Resistor of 2kΩ, an Inductor of 2nH, a linearly graded pn junction and an npn BJT?	2	CO3
	(iv)	Drawing the energy band diagrams specify: onset of inversion and strong inversion conditions for a MOSFET. Compute different parameters from these energy band diagrams.	2	
	(v)	Enlist the different nomenclatures for high speed FETs and give the working principle of these transistors.	2	
2.	(i)	Evaluate the performance of a BJT and a MOSFET in a tabular way from fabrication, working and applications, point of view.	2	CO4
	(ii)	Draw the electrical equivalent model of a pn junction diode. Hence develop an Ebers Moll ac equivalent circuit model of a BJT and highlight its importance.	3	CO2
	(iii)	At 300K, let the normal (β_N) and inverse (β_I) mode common emitter current gains be 100 and 2, respectively, for a BJT. For an emitter bias of 0.7V, the normal mode emitter current is 5mA. Determine the emitter (I_{ES}) and collector (I_{CS}) saturation currents. It is known that $\alpha_N I_{ES}=\alpha_I I_{CS}$.	5	CO4
3.	i)	Design a step p+n junction diode at room temp to attain a built-in potential of 0.35V.	5	CO2
	ii)	Analyze which of the following MOSFETs, MODFETs and MESFETs is the most important transistor and justify it?	5	CO4
4.	i)	Derive a relationship to show the effect of charge sharing on threshold voltage in short channel MOSFETs. How is threshold voltage varied in a narrow channel device?	5	CO2
	ii)	Develop an electrical equivalent model of a MOSFET. Enlist reasons why such a model is essential for semiconductor devices and circuit simulation?	5	CO1

P.T.O.

5.	i)	If input pulse signal is of 0V & 1V initial and final values, and rise & fall times are 2ns, respectively; initial delay can vary from 5 to 10ns, pulse width is 20ns and pulse period is 40ns. Write down the SPICE netlist for transient analysis till 100ns of a CMOS inverter driving a capacitive load of 0.1pF. Draw the circuit, the expected input and output waveforms. Let CMOS technology node be 90nm, use 5times the minimum dimensions of transistors and supply voltage 1V.	**5**	CO3
	ii)	Design and analyze a MESFET to work in depletion mode.	**5**	CO4

$DATA: \varepsilon_o = 8.854\times10^{-12} F/m, \varepsilon_{ox} = 4, \varepsilon_{Si} = 12, n_i = 1.5\times10^{16} m^{-3}, k = 1.38\times10^{-23} J/K,$

$R = (np - n_i^2)/[\tau_n\{p + n_i \exp((-(E_t - E_i))/kT)\} + \tau_p\{n + n_i \exp((E_t - E_i)/kT)\}]$