Dr S.K Soni
20/11/23

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Roll No.: .....

National Institute of Technology, Hamirpur(HP)
Electronics & Communication Engg. Deptt
End Semester Examination December 2023

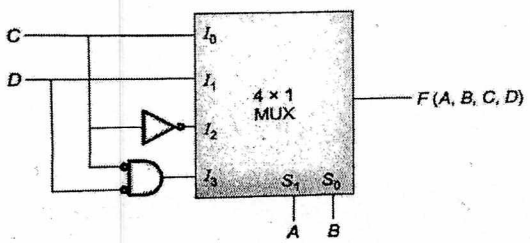
Branch : ECE, CSE, EE
Course Name : Digital Electronics & Logic Design
Time: 03:00 Hours
Note: All questions are compulsory.

Semester : 3rd semester
Course Code: EC-211
Maximum Marks: 50

SECTION – A

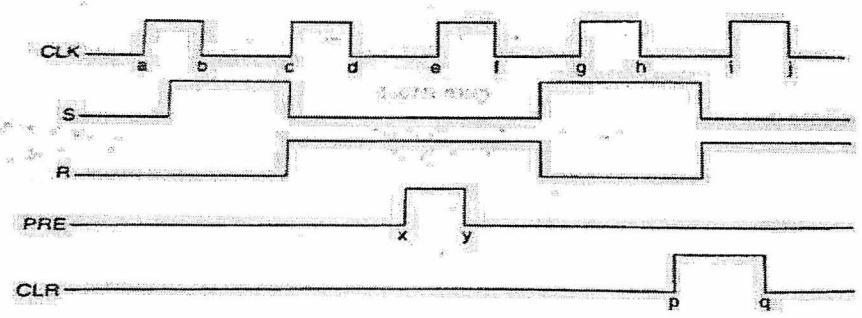
(Question 1 to 10 carry 3 marks each.)

1. Consider a number systems having digits, 0,1,2,A,B,C. Perform the following operations:
   (i) 0ABC-C2B1
   (ii) 0ABC+C2B1
2. (i). if $(292)_{10}=(204)_b$, then what is the possible value of b .
   (ii) Perform the BCD subtraction of 77-64
3. Find the Boolean function (in terms of minterms) realized by the logic circuit shown in Figure below.



4. An 8-bit SA type ADC has a resolution of 15 mV. What will be its digital output for an analog input of 2.65V.
5. Draw and explain the logic circuit of 2 input NOR gate using CMOS logic.
6. Implement function f(A,B,C) = ∑m(0,2,4,6,7) using 4:1 mux by choosing BC as select line.
7. Minimize the function F(A,B,C,D)=∑m (0,1, 8, 9,13,11, 14) with Quine- McCluskey method and implement with NAND gates only.
8. Implement the following pair of Boolean expressions: $F_1(A,B,C)= \prod(1,3,4,5)$, $F_2(A,B,C)= \sum(1,2,4, 5)$ using 3:8 decoder.

9. The waveforms shown in Figure given below are applied to negative edge triggered J-K flip flop with active-HIGH PRESET and CLEAR. Draw the output waveform of the flip flop.



10. It is desired to construct a combinational circuit which will give an output Y=1 only when the input 4 bit binary number ABED denote month which has 31 days. The months are coded such that ABCD=0001 denoted January, 0010 denotes February....., 1100 denoted December. Only those inputs are allowed which actually denotes some month

i) Write the truth table in terms of input variable ABCD.

ii) Find out the minimized expression and build the circuit using NAND gates only.

SECTION – B

(Question 11 to 15 carry 5 marks each.)

Attempt any four

11. Show how the PLA circuit with three input variable and four outputs would be programmed to implement the full adder and full subtractor circuit.

12. Design a synchronous counter using T flip flop to count in the following sequence
0, 2, 3, 4
Check whether it is a self starting circuit or not.

13. Explain the characteristic parameters of digital logic families. Explain the circuit and working of 3 input NAND transistor-transistor logic gate.

14. Consider a PN flip-flop having four operations, reset to 0, hold, complement and set to 1, when inputs PN are 00, 01, 10, 11 respectively. Tabulate the characteristic table, excitation table and show how the PN flip-flop can be converted to a D flip-flop.

15. Design a sequence detector circuit which is to provide an output equal to 1 whenever any of the following input sequence is detected: 1101, 1001