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Architecture of Large Systems

Subject code: CS-613 Nov-2023

Max Time: 3:00 hr **Max Marks: 50**

Note: **All** questions are **compulsory**. Assume necessary data (if required).

Q.1. Consider the following statement:

a) A program contains 20% of non-parallelizable code and the remaining being fully parallelizable. How many processors are required to achieve a speedup of 3? Is it possible to achieve a speedup of 5? What do you infer from this?

b) Is it possible to solve an arbitrary large problem in a fixed amount of time, provided that unlimited processors are available? Why? **2.5+2.5=5**

Q.2. Our favorite program runs in 10 seconds on computer A, which has a 4 GHz clock. We are trying to help a computer designer build a computer, B that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? **5**

Q.3. What are the different types of hazards? Explain by taking a MIPS processor example. **5**

Q.4. In the instruction set of a RISC processor, there are 25 instructions, and 32 registers in the bank of registers. What will be the minimum length (in bits) of encoded instructions and why? The instruction set contains arithmetic instructions like add, immediate type instructions and jump type instructions. Explain your answer in brief. How does your answer change for a processor with accumulator organization? **5**

Q.5. What do you mean by Multiway interleaved memory organization? Draw a diagram for four-way high-order interleaving memory. Consider length of logical address according to your convenience. **5**

Q.6. Explain the data path of MIPS with instruction format (at least two examples for each instruction type). **5**

Q.7. Consider the following assumption bisection bandwidth?

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1 = 25$ ns	$s_1 = 512$ Kbytes	$c_1 = \$1.25$
Main memory	$t_2 =$ unknown	$s_2 = 32$ Mbytes	$c_2 = \$0.2$
Disk array	$t_3 = 4$ ms	$s_3 =$ unknown	$c_3 = \$0.0002$

Total cost of the memory should not exceed \$15,000. What will be the t_2? **5**

Q.8. What do you understand by pipelining? What are the different hindrances to ideal pipelining? What are these hindrances called? How can you remove such hindrances? Explain with help of suitable examples for each part of your answer. **5**

Q.9. Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-

1. Number of bits in tag
2. Tag directory size

5

Q.10. Explain the Cache Memory Organization and its types. How cache is associated with physical address/ virtual address. Support your answer with diagram. **5**