Dr. Dharmendra Singh Yadav

12/5/2023 (E)

Name: Roll No. 234

NATIONAL INSTITUTE OF TECHNOLOGY HAMIRPUR (HP)

End –Semester Examination, May 2023

Branch: B. Tech (E&CED) **Year:** 4th Year
Course Name: Analog VLSI Design **Semester:** 8th
Course Code: EC-642 **Time:** 3 Hrs
Max Marks: 50

NOTE: All questions are compulsory.

Question 1(a). Explain the Analog Design Challenges in term of imperfections, supply voltages, power, complexity, and variation in PVT (Process, Voltage, and Temperature). **[5]**

Question 1(b). For Fig. 1, plot the on-resistance of M1 as a function of V_G. Assume that $\mu_n C_{ox}$ = 50 $\mu A/V^2$, W/L = 10, and V_{TH} = 0.3 V. (Note that the drain terminal is open) **[2]**

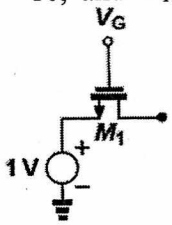

Fig.1.

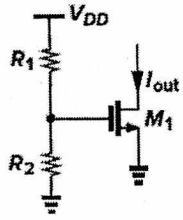

Fig.2.

Question 2 (a). (i) For the given Equation suggests that if V_{SB} becomes negative, then V_{TH} decreases. Is this correct? **[3]**

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\emptyset_f + V_{SB}} - \sqrt{|2\emptyset_f|}\right)$$

(ii) Explain the channel length modulation and write down the basic current equations for triode and saturation region by considering the effect of channel-length modulation.
(iii) Is there channel-length modulation in the triode region?

Question 2 (b). For W/L = 50/0.5, plot the drain current of an NMOS and a PMOS as a function of $|V_{GS}|$ as $|V_{GS}|$ varies from 0 to 3 V. Assume that $|V_{DS}|$ = 3 V. **[5]**

Question 3 (a). In Fig. 2, assume that $(W/L)_1$ = 50/0.5, λ = 0, I_{out} = 0.5 mA, and M1 is saturated.
(i) Determine R_2/R_1. **[5]**
(ii) Calculate the sensitivity of Iout to V_{DD}, defined as $\partial I_{out}/\partial V_{DD}$ and normalized to I_{out}.
(iii) How much does Iout change if V_{TH} changes by 50 mV?
(iv) If the temperature dependence of μ_n is expressed as $\mu_n \propto T^{-3/2}$ but V_{TH} is independent of temperature, how much does I_{out} vary if T changes from 300K to 370K?

Question 3 (b). Calculate the gain of given circuit in Fig. 3 at very low and very high frequencies. Neglect all other capacitances and assume that $\lambda = \gamma = 0$. **[5]**

OR

Question 3 (c). Calculate the gain of given circuit in Fig.4 at very low and very high frequencies. Neglect all other capacitances and assume that $\lambda = \gamma = 0$.

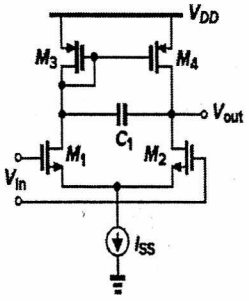

Fig.3.

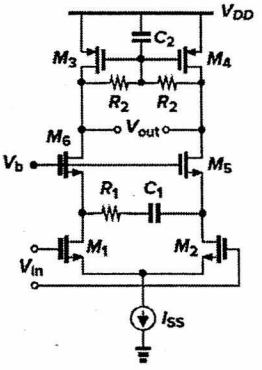

Fig.4.

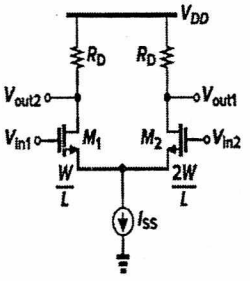

Fig.5.

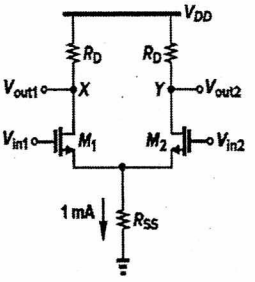

Fig.6.

Question 4. Explain Voltage -Voltage Feedback? Derive the formula of loop gain and calculate the output resistance. **[5]**

OR

Explain Current -Voltage Feedback? Derive the formula of loop gain and calculate the output resistance.

Question 5. Due to a manufacturing error, in the circuit of Fig.5, M2 is twice as wide as M1. Calculate the small-signal gain if the dc levels of V_{in1} and V_{in2} are equal. **[5]**

Question 6. The circuit of Fig.6. uses a resistor rather than a current source to define a tail current of 1mA. Assume $(W/L)_{1,2}=25/0.5$, $\mu_n C_{ox}=50\ \mu A/V^2$, $V_{TH}=0.6V$, $\lambda=\gamma=0$, and $V_{DD}=3$ V.
(a) What is the required input CM voltage for which R_{SS} sustains 0.5 V? **[5]**
(b) Calculate R_D for a differential gain of 5.
(c) What happens at the output if the input CM level is 50 mV higher than the value calculated in (a)part?

Question 7(a). When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50. **(i)** Calculate the fraction of the output voltage feedback. **(ii)** If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75. **[5]**

OR

Question 7(b). The gain of an amplifier without feedback is 50 whereas with negative voltage feedback, it falls to 25. If due to ageing, the amplifier gain falls to 40, find the percentage reduction in stage gain **(i)** without feedback and **(ii)** with negative feedback.

Question 8. Explain the following by using op-amp:- **[5]**
(a) The Differential Amplifier
(b) The Inverting Amplifier
(c) The non-inverting amplifier
(d) Voltage Follower
(e) Concept of virtual short circuit

**********ALL THE BEST**********