Dr Gargi Khanna 178 8/5/2023

Roll No.: .....

National Institute of Technology, Hamirpur(HP)

Name of Examination: B.Tech (May-2023)

Branch: **Electronics & Comm. Engineering** Semester : 8th
Course Name: **Low Power VLSI Design Techniques** Course Code: **EC-461**
Time: **3Hours** Maximum Marks: **50**
Note: **All questions are compulsory.**

1. a) What do you mean by precomputation logic?

   b) Design a scaled chain of inverters such that the delay time between the logic gate input(Cg = 20 fF) and a load capacitance 2 pF in minimized.

   c) Compare performance of two transistors with subthreshold slope of 60mV/decade and 100mV/decade.

   d) Describe the causes for glitching power dissipation.

   e) What is slack time? How it is important for implementation of Duel Vt technique.

   e) Define skew and jitter in clock distribution network.

(2*6)

1. Describe the propagation of static probability and transition density in logic circuits. Write down the algorithm for gate level power analysis for combinational circuits using these statistical parameters. Find out the transition density of output of 2:1 multiplexer circuit static probabilities of the inputs A,B and select line S are 0.1, 0.2, 0.3 and transition density of inputs are 4,3 and 5 respectively.

(8)

2. a) Describe the circuit and working of a self clock gating positive edge triggered transmission gate Flip Flop.

b) Design a circuit for implementation of function
$F = \overline{A.(B+C) + D.E}$
Using compound gate logic with minimum delay. Calculate the minimum delay of your design when there is a maximum input capacitance of 15 units on each input and output load capacitance is of 150 units

(5, 5)

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3. a) Describe the statistical approach to define the stopping criteria and MONTE CARLO power simulation process. The standard deviation of the power samples has been observed to have ±10% fluctuation from the mean. How many samples are required so that 95% confidence that error of sample mean is within ±5%. How many more samples are required if confidence level is 99% .

   b) Describe the need and concept of bus invert encoding for low power dissipation.

   (5, 5)

4. a) Describe and find out the short circuit power dissipation. List down all the assumption considered. Explain the short circuit current variations with input signal slope and output load.

   b) Describe the method of Datapath module characterization for the power analysis at the architectural level. Explain the model used for the analysis of multibit adder.

   (5, 5)