Prof Rajeev Arora

Roll No.:..... 1/5/2023

National Institute of Technology, Hamirpur (HP)

Name of Examination: **END-SEMESTER** Examination
Branch: B.Tech. & Dual Degree ECE 3rd Year
Course Name: VLSI Design Techniques
Time: 3 Hours

Session: 1 May 2023
Semester: 6th
Course Code: EC-323
Maximum Marks: 50

Note: *All questions are compulsory and carry equal marks. Assume any missing data.*

1	(a)	Draw voltage transfer characteristics (VTC) of CMOS and NMOS inverters. Which region of the VTC is used for digital and analog circuit designs and why?	5+5
	(b)	A CMOS inverter has V_{IL}=1.2V, V_{IH}=1.6V, V_{DD}=3.3V. When input is 1.2V, output is 3.1V. The threshold voltages for NMOS and PMOS are V_{tn}=0.5V, V_{tp}= -0.6V, respectively. Determine the logic threshold voltage of the inverter.	
2	(a)	If frequency of operation is 1MHz, C_L=1pF, K=10μA/V^2, I_0=I_{sub}=1nA, T=0.1T, V_{DD}=5V, switching activity α_t=1 and V_t=0.2V, determine the power components and the total power dissipation in a CMOS inverter.	5+5
	(b)	Workout the drain-gate capacitance of the MOSFET in saturation and linear regions if C_{ox}= 5.5x10^{-3} F/cm^2, for W=3λ, L=2λ, L_D= λ/4, if technology=1μm.	
3	(a)	Identify the main problems encountered in precharge-evaluate logic and suggest suitable remedies for these problems. **OR** Give schematic circuit of a 3-input dynamic NAND gate. If the parasitic capacitances double from bottom, what is the percentage extent of charge sharing?	5+5
	(b)	For a CMOS inverter, V_{DD} =5V, Channel length=1μm and C_L= 2pF. V_{tn}=0.8V, V_{tp}=-1V, K_n'=50μA/V^2 and K_p'=20μA/V^2. Design the inverter by determining the channel widths of the two transistors for an inverter threshold voltage of 2.2V and propagation delay T_{pHL}=5ns.	
4	(a)	What are the meanings and significance of the parameters g_o and g_m in analog VLSI design? Determine their relationships using Shichman Hodges or MOS level-1 models, for linear and saturation regions of MOS transistor operation.	5+5
	(b)	Determine the gain of a single stage common source MOS amplifier.	
5	(a)	Design a 4x4 NAND **or** NOR based ROM memory, giving proper schematic diagram.	5+5
	(b)	Design an equivalent CMOS inverter circuit for function Y, if all PMOS and NMOS are of the same dimensions. Identify the possible Euler's path solutions for Y and draw the stick diagram for any one of the possible solutions. Given the function, Y = Bar {(A+BC)DE}.	