Ashwani Rana,

National Institute of Technology, Hamirpur (HP) Name of Examination: B. Tech. (May-2023)

Branc Cours		me : ECE : VLSI Technology	Semester : Course Code :	4 th EC-224	
Time	3 H	ours	Maximum Marks: 5		
Note:	1) A	ttempt all the questions.	NATIO: 3	·	
·	2) A:	ssume suitable data if required			
Q (1):	a)	What are the requirements of silicon wafer for electron which such silicon can be produced. List their advantage a	nics Industry and explain atle	east two methods by	y (5)
	b)	as a solution reading the gate 0x10e of M(1) Device & why? E1-1			(5)
Q (2):	a)	Determine the diffusivity of the phosphorous diffusion carried out for 1 hour into an activity			l (5)
	b)	Why is Ion-implantation preferred over diffusion for intechnique.	npurity doing? Explain brie	fly ion-implantation	(5)
Q (3):	a)	Describe in detail the Sputter ion plasma technique for etching the dielectric layer. Discuss its various merits and demerits over other etching techniques.			(5)
	b)	Draw a schematic of a planner reactor used for Reactive Ion your observation if CF ₄ /H ₂ is used in RIE in place of CF ₄ /O	on Etching and explains the process in detail. Give O_2 .		
Q (4):	a)	741 op-amps have been fabricated using a 2µm technology on a silicon wafer. Describe the various processes involved in the packaging of above op-amp using 8-pin plastic cases.		(5)	
	b)	Why is it economical to fabricate diodes from transistors in fabricated from transistor?	n IC technology? If it is true,	how can diodes be	(5)
		OR			(0)
		Describe the fabrication processes for fabricating PNP BJT			
Q (5):	a)	Describe the fabrication of monolithic resistors and capacitor using bipolar technology. (5)			(5)
	b)	How components are electrically isolated in Monolithic IC's	?		(5)