Dr Sangeeta Sharma 6/5/2023

Name of student: Scholar No.:

National Institute of Technology Hamirpur
Department of Computer Science & Engineering
End-Semester Exam May-2023

Branch: B.Tech (CSE) 4th Sem
Subject: Computer Organization and Architecture **Max Marks: 50**
Code: CS-221 **Max Time: 03:00 hrs**

Note: 1. All questions are compulsory.
2. Draw neat diagrams wherever necessary.
3. Direct answers will not be evaluate, only completely described answers will be consider.
4. In case of any confusion in any terminology, preference will be given to whatever has been taught in the class.
5. Handwriting should be clean. The answers will not be checked if handwriting is not legible.
6. Write all the answers in the sequence of question numbers.

Q.1 What is goals of Parallelism. Explain pipelining and its properties. What are the different types of pipelining? What are the different major difficulties that cause the instruction pipeline to deviate from its normal operation, explain? [10 Marks]

Q.2 Describe all three types of methods for data transfer between the central computer and I/O devices i.e. Programmed I/O, Interrupt-initiated I/O, and Direct memory access (DMA). [9 Marks]

Q.3 What do you mean by memory hierarchy. Explain cache memory and its properties. Why cache mapping is required. Describe different cache mapping techniques. [9 Marks]

Q.4 Explain cache coherence problem in multiprocessor system. What are different conditions for incoherence? Explain with example and give the possible solutions to the Cache Coherence Problem. [6 Marks]

Q.5 Give whether the following statements are true/false with proper explanation. [4 Marks]
a) Mapping in the fully associative cache is faster than a direct mapped cache of the same size.
b) The number of blocks in a direct mapped cache should be a power of 2.
c) The number of bytes in a cache block should be a power of 2.
d) In the write through policy, data in memory is always consistent with data in cache.

Q.6 A 2-way set associative write back cache with true LRU replacement requires 15 bits to implement its tag store per set (including 1 bit for LRU, 2 bit for Dirty and 2 bit for Valid). The cache is physically indexed, physically tagged and cache contains 512 blocks of each of size 8 bytes and is byte addressable. What is the physical address space in (Kbytes) of this memory system? [3 Marks]

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Q.7 Consider a cache works at 5 X speed of main memory with hit rate of 75%. What is the speedup of the memory performance if such cache is used? Assume that parallel searching is performed in both cache and memory. [3 Marks]

Q.8 Consider a computer with the following characteristics: [3 Marks]

- Total of 4 MB of main memory;
- Word size of 2 bytes;
- Block size of 32 bytes;
- Cache size of 128 Kbytes;
- Assume the memory is word addressable.

What is the corresponding tag, cache line address, and word offsets for a direct-mapped cache?

Q.9 Consider the following assembly code: [3 Marks]

1. add R2, R5, R4 // R2 = R5 + R4
2. add R4, R2, R5 // R4 = R2 + R5
3. sw R5, 100(R2) // Mem[R2] = R5
4. sub R3, R2, R4 // R3 = R2 - R4

From the above instructions, which of the pair of instruction does not require data forwarding in a 5-stage RISC pipelined processor?