Dr Kodandaram M. 12/12/2022

(15) (25)

National Institute of Technology Hamirpur

Department of Electronics and Communication Engineering

B.Tech ECE Dual Degree

End Semester Examination – Nov 2022

Course :VLSI TEST AND TESTABILITY — *Course number : EC-737*

VII Semester — ***Answer all questions*** — Maximum marks : 50

1. What is fault simulation? Explain different types of fault simulations (4)
2. Mention basic steps involved in implementing D-algorithm. Find suitable test vector for SA-0 at u using D-algorithm in Fig.1 (6)

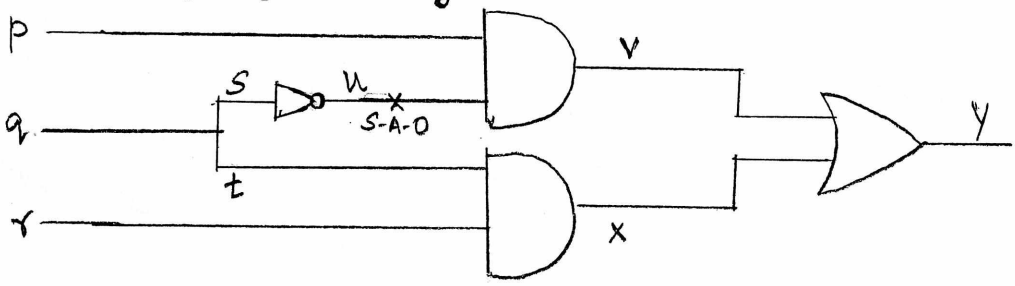

Fig.1

3. a) Define terms controllability and observability. (4)
   b) How are DFT techniques categorized? Explain Ad hoc techniques. (5)
4. a)Find suitable test vector to detect y s-a-0 in Fig.2 using PODEM method (6)

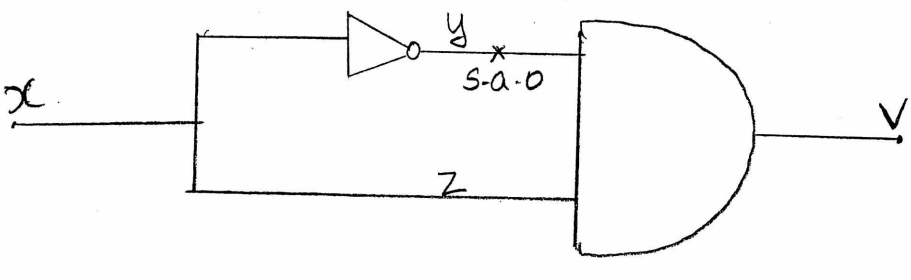

Fig.2

b) Write the difference between FAN and PODEM methods. (4)

(P.T.O)

5. Design a 4 stage standard LFSR for polynomial $P(x) = 1+x+x^4$.Generate maximal length pseudorandom pattern assuming initial value for LFSR as 0001. (5)

6. Explain BIST and its classification with neat diagram. (6)

7. a) Find the test set to determine the S-A-0 fault at node h in the Fig.3(a) using Boolean difference method (5)

   b) Find test vector to test S-A-0 fault at node Z in Fig.3 (b) using Boolean Difference method. (5)

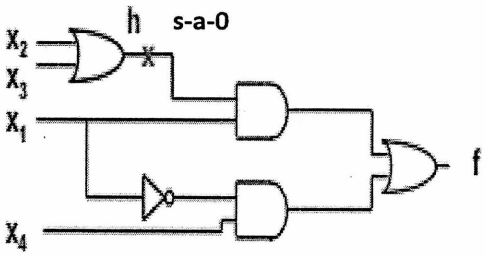

Fig .3 (a)

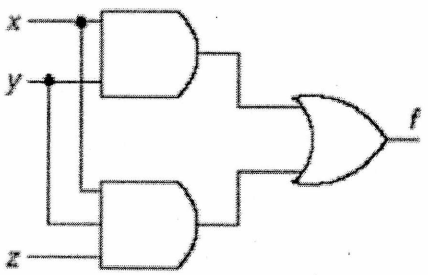

Fig .3 (b)