Prof Rajeev Chauhan (27) 30/11/2022

Roll No.:...................

# National Institute of Technology, Hamirpur (HP)

**Name of Examination:** END-SEMESTER EXAMINATION, Nov 2022

**Branch:** Dual Degree Integrated E&CE | **Semester** : 7th

**Course Name:** Device Modeling for Circuit Simulation | **Course Code** : EC-631

**Time:** 3 Hours | **Maximum Marks:** 50

**Note:** All questions are compulsory and carry equal marks. Assume missing data if any.

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|---|---|---|---|
| 1. | (a) | Develop electrical model of a PN junction diode. | 2 |
| | (b) | What is the significance of electronic device modeling for circuit simulation? | 3 |
| | (c) | For a CMOS inverter driving a capacitive load of 0.2pF, provide SPICE netlist for determining the transient analysis. The supply voltage is 2V. Consider minimum size NMOS FETs for 180nm technology node. Given input pulse signal has 0V and 2V initial and final values, initial delay is 10ns, rise and fall times are 5ns each, pulse width is 50ns and pulse period is 100ns. Draw the circuit and the expected waveforms for two time-periods. | 5 |
| 2. | (a) | Derive level-1 MOS model? What are its main limitations? Name the model which overcomes these? | 5 |
| | (b) | Give MOS capacitance model. Given the drawn gate-length of a MOSFET is 2μm. The Source/Drain overlap is 0.2μm each. The gate width is 20μm. The thickness of the gate-oxide of the device is 20nm. Determine the value of the gate-source capacitances of the device for cut-off, linear and saturation regions. | 5 |
| 3. | (a) | Enlist and brief-up the short-channel and narrow channel effects that crop-up in highly scaled MOS transistors? | 5 |
| | (b) | For an NMOS the drawn gate length is 2μm and width is 20μm. The Gate to Source and Gate to Drain overlaps are 0.2μm each. The transconductance parameter (K') of the MOSFET is $60\mu A/V^2$. The gate oxide capacitance is $2x10^{-4}F/m^2$ and substrate permittivity is 12. The intrinsic carrier concentration of silicon is $1.5x10^{16}/m^3$ at 300K. The substrate doping is $5x10^{21}/m^3$ and channel length modulation parameter is $0.02V^{-1}$. Silicon gate technology is used for gate formation. The surface or oxide charge density is $2x10^{-4}$ $C/m^2$. Determine the Drain current at (i)0.5V and (ii)5V drain voltages, for a gate bias of 5V.<br>**OR**<br>Using energy band diagrams show the concept of threshold voltage ($V_t$) in MOS devices. Derive the relationships for zero and non-zero bias $V_t$. | 5 |
| 4 | (a) | Give pros and cons of BJTs and MOSFETs in a tabular form, with suitable figures where ever needed. | 5 |
| | (b) | Explain the concept of Ohmic and rectifying contacts. Hence, write about the two types of MESFETs. | 5 |
| 5 | (a) | Discuss Ebers-Moll dc and ac models of a BJT. | 5 |
| | (b) | Highlight the main features of 2D electron gas, GaAs and $Al_xGa_{1-x}As$? Giving schematic structure, explain the principle of a HEMT or TEGFET | 5 |

$DATA: \varepsilon_o = 8.854\times10^{-12} F/m, \varepsilon_{ox} = 4, \varepsilon_{Si} = 12, n_i = 1.5\times10^{16} m^{-3}, k = 1.38\times10^{-23} J/K,$

$R = (np - n_i^2)/[\tau_n\{p + n_i \exp((-(E_t - E_i))/kT)\} + \tau_p\{n + n_i \exp((E_t - E_i)/kT)\}]$