National institute of Technology Hamirpur (H.P.)
Electronics & Communication Engineering Department
Course Code: EC – 211
Course Name: Digital Electronics & Logic Design
Branch: B.Tech, CSE
End Semester Online Exam. December 16, 2020

Time: 120 Minutes **Maximum Marks: 50**

Note: 1. All questions are compulsory.

2. Write your roll number, name, course code, subject name on top of every sheet and signature with date on the bottom of every sheet of your answer sheet.

1. a) Implement full subtractor circuit with 4:1 multiplexer circuit only.

b) Minimize the following function by using Quine McKlusky method:

F(W,X,Y,Z) = ∑m(_, _, _, _, _, _ , 10,13) Fill in the blanks with the digits of your roll number. Implement minimized function using NAND gates only.

(6, 6)

2. a) Design a circuit that compares two binary numbers X and Y, each having two bits (X = x1x2; Y=y1y2). It has a single output C which is supposed to be 1 when X > Y, and 0 otherwise. Draw the minimum sum-of-products circuit using the correct circuit symbols for all gates. Assume complemented gates are not available, but multiple input gates are. What is the delay of the circuit, assuming the delay for each gate is d?

b) Implement a three input NAND gate using CMOS logic.

(6, 6)

3. a) Design a MOD 8 synchronous up counter using T flip flop

b) Design a MOD 10 asynchronous counter using D flip flop.

(6, 6)

4. a) Design a 1:4 Demultiplexer circuit. Realize the following function using 1:16 demultiplexer while connecting variables to the select lines:

F (a,b,c,d) = ∑m(_, _, _, _, _, _ , 10,13,15) Fill in the blanks with the digits of your roll.

b) Design a BCD to excess three code converter using Programmable Logic Array.

(7, 7)